APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,420	03/20/2001	Stephen Allott	1875.8080000	2396

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EXAMINER
BHATTACHARYA, SAM

ART UNIT	PAPER NUMBER
2617	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/813,420	ALLOTT ET AL.
	Examiner	Art Unit	
	Sam Bhattacharya	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>21 August 2006</u>.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>2-10</u> is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) <u>7</u> is/are allowed.

6)☒ Claim(s) <u>2-6 and 8-10</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All   b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
　　Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
　　Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.　　　The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2.　　　Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luz et al. (US 6,321,073) in view of Nielsen (US 6,985,518).

　　　As to claim 2, Figures 1 and 2 in Luz show a radio receiver (100) (see Col. 2, lines 40-67), comprising:

　　　an amplifier (104a, 104b, 104c) configured to receive and amplify an intermediate frequency modulated signal having in-phase and quadrature phase DC components;

　　　an analog-to-digital converter (110) configured to receive the amplified intermediate frequency modulated signal and convert it to a digital signal;

　　　a demodulator (202) operable to demodulate the digital signal; and

　　　DC offset calibration means (202) coupled to the demodulator operable to provide in-phase and quadrature phase DC offset correction signals to compensate for the in-phase and quadrature phase DC components at the input of the amplifier ("the feedforward DC offset compensation circuit 202 generates an in-phase digital error signal 360a (see FIG. 3A) and a quadrature phase DC error signal 360b to remove DC offsets introduced by the ADC or other sources. These signals are combined and subtracted from the signal" (Col. 3, lines 10-14)).

　　　Luz fails to disclose delay measurement means coupled to the demodulator operable to determine a delay vector.

However, in an analogous art, Nielsen discloses a receiver including delay measurement

means 32 coupled to the demodulator 36 operable to determine delay vectors. See FIG. 2 and

col. 4, lines 7-45. Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify the receiver in Luz by incorporating the above-noted

features taught in Nielsen for the purpose of determining correction values to compensate for

directional components of the offset signal.

As to claim 3, the Luz reference discloses the radio receiver of claim 2, wherein the delay

vector is used by the DC offset calibration means to provide a digital representation of the in-

phase and quadrature phase DC offset correction signals ("Each of these results is truncated into

a 20-bit results in truncators 358a and 358b. The result is a DC offset error 360a for the in-phase

signal and a DC offset error 360b for the quadrature phase signal" (Col. 4, lines 35-38). See also

Col. 4, lines 20-35).

As to claim 4, Luz (Figure 3b) discloses the radio receiver of claim 3, further comprising:

a first digital-to-analog converter (386) configured to receive a in-phase component of the digital

representation of the in phase DC offset correction signal for mixing with an in-phase signal and

an intermediate frequency carrier signal; a second digital-to-analog converter (388) configured to

receive a quadrature phase component of the digital representation of the quadrature phase DC

offset correction signal for mixing with a quadrature signal and the intermediate frequency

carrier signal ("the gain control 384 is input to digital analog converters 386 and 388

simultaneously so that gain control is applied to all gain stages at the same time" (Col. 5, lines 1-

3)); and

a summer operable to subtract the mixed quadrature phase signal and quadrature phase

DC offset correction signal component from the mixed-in phase signal and in-phase DC offset

correction signal to provide a DC compensated intermediate frequency modulated signal at the

input of the low noise amplifier ("these DC offset errors 360a and 360b are combined in an error

combiner 362 and a net offset error 364 is subtracted in substractor 332 with the signal 330 to

obtain a DC compensated input signal 366" (Col. 4, lines 38-41)).

3.   Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent

6,321,073 to Luz et al. in view of Nielsen (US 6,985,518) and Galal et al. (U.S. Patent

6,161,004).

As to claim 5, the Luz reference (Figures 1 and 2) discloses a radio receiver (100) (see

Col. 2, lines 40-67), comprising:

an automatic gain control stage (104a, 104b, 104n) coupled to the summer and operable

to amplify the integrated signal;

an analog-to-digital converter (110) operable to convert the amplified integrated signal to

a digital signal;

a demodulator (202) operable to demodulate the digital signal; and

Luz fails to disclose delay measurement means coupled to the demodulator operable to

determine a delay vector.

However, in an analogous art, Nielsen discloses a receiver including delay measurement

means 32 coupled to the demodulator 36 operable to determine delay vectors. See FIG. 2 and

col. 4, lines 7-45. Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify the receiver in Luz by incorporating the above-noted features taught in Nielsen for the purpose of determining correction values to compensate for directional components of the offset signal.

The combination of Luz and Nielsen does not disclose a receiving stage configured to receive a radio signal; a first mixer stage operable to downconvert the radio frequency signal to a first intermediate frequency in-phase signal and a first intermediate quadrature phase signal; first and second low pass filters configured to receive and low pass filter the first intermediate frequency in-phase and quadrature phase signals; a second mixer stage operable to upconvert the filtered first intermediate frequency in-phase and quadrature phase signals and provide a second intermediate frequency in-phase signal and a second intermediate frequency quadrature phase signal; and a summer operable to subtract the second intermediate frequency quadrature phase signal from the second intermediate frequency in-phase signal to provide an integrated signal;

The Galal reference teaches a receiving stage configured to receive a radio signal; a first mixer stage operable to downconvert the radio frequency signal to a first intermediate frequency in-phase signal and a first intermediate quadrature phase signal; first and second low pass filters configured to receive and low pass filter the first intermediate frequency in-phase and quadrature phase signals; a second mixer stage operable to upconvert the filtered first intermediate frequency in-phase and quadrature phase signals and provide a second intermediate frequency in-phase signal and a second intermediate frequency quadrature phase signal; and a summer operable to subtract the second intermediate frequency quadrature phase signal from the second intermediate frequency in-phase signal to provide an integrated signal (see Figure 18 and Col. 10, line 8 to Col. 11, line 56).

Therefore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to modify the device of Luz and Nielsen to comprise a receiving stage

configured to receive a radio signal; a first mixer stage operable to downconvert the radio

frequency signal to a first intermediate frequency in-phase signal and a first intermediate

quadrature phase signal; first and second low pass filters configured to receive and low pass filter

the first intermediate frequency in-phase and quadrature phase signals; a second mixer stage

operable to upconvert the filtered first intermediate frequency in-phase and quadrature phase

signals and provide a second intermediate frequency in-phase signal and a second intermediate

frequency quadrature phase signal; and a summer operable to subtract the second intermediate

frequency quadrature phase signal from the second intermediate frequency in-phase signal to

provide an integrated signal, as taught by Galal, in order to implement a dual path mixing

network to provide for balanced gain and group delay distortion among the upper and lower

paths of the mixing network.

As to claim 6, Luz-Nielsen-Galal discloses the radio receiver of claim 5. The Luz

reference further teaches: a DC offset calibrator coupled to the delay measurement means (see

Col. 4, lines 20-38); an in-phase digital-to-analog converter coupled between the DC offset

calibrator and the second mixer stage; and a quadrature phase digital-to-analog converter coupled

between the DC offset calibrator and the second mixer stage, wherein the in-phase digital-to-

analog converter is operable to provide an in-phase DC offset compensation signal for the

automatic gain control stage and the quadrature phase digital-to-analog converter is operable to

provide a quadrature phase DC offset compensation signal for the automatic gain control stage

("the gain control 384 is input to digital analog converters 386 and 388 simultaneously so that

gain control is applied to all gain stages at the same time" (Col. 5, lines 1-3). See also Col. 4,

lines 38-67).

4.   Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S.

Patent Application Publication 2002/0114413 A1 to Zarubinsky et al. in view of Nielsen and

Galal et al. (U.S. Patent 6,161,004).

As to claim 8, the Zarubinsky reference discloses a method of compensating for DC

offset voltages present at an input of a low noise amplifier, the method comprising the steps of:

determining a signal delay between an output of a second mixer stage of the dual mixer

stage radio receiver, said signal delay characterizing in phase and quadrature phase components

of the DC offset voltage present at the input of the low noise amplifier ("delay stage 207

forwards signal X'_D with a delay of N time slots T. The symbol Z_{-N} is an operator of a Z-

transformation. Persons of skill in the art can implement delay stage 207 with out the need of

detailed explanation herein, for example, by a shift register. The delay of stage 207 conveniently

corresponds to the intrinsic input-to-output delay introduced in in-phase channel 291 (e.g., by

DAC 293, LPF 295. This is convenient. As explained in connection with FIG. 3, the "input

related" signal X_D is combined with the delayed "output related" X_A (page 5, col. 1, paragraph

[0077]));

using the determined signal delay to separate and define digital representations of the in-

phase DC offset voltage component and the quadrature phase DC offset voltage component

("FIG. 9 illustrates a simplified block diagram of offset compensation control loop 401" (page 5,

col. 2, paragraph [0094], lines 1-2). "Integrator 441 obtains an estimation of the magnitude and

feeds back a compensation offset signal OCOMP (P,P) to either one of the inputs of

corresponding digital comparator 221. In the example of FIG. 9, this implemented by subtracting

OCOMP (P,P) form ID(P) by subtractor 411. Delay stage 431 delays by the delay time

introduced by channel 292" (page 5, col. 2, paragraph [0095]));

making the digital representation of each of the in-phase and quadrature phase

components more positive or more negative if it is more negative or more positive than a

predetermined minimum threshold or maximum threshold; and performing the above sequence

of steps a predetermined number of times to reduce the DC offset voltage at the input of the low

noise amplifier (see page 6, col. 1, paragraphs [0097] and [0098]).

Zarubinsky fails to disclose that the determination of the delay has component delay

vectors. However, in an analogous art, Nielsen discloses a receiver including delay measurement

means 32 coupled to the demodulator 36 operable to determine delay vectors. See FIG. 2 and

col. 4, lines 7-45. Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify the receiver in Luz by incorporating the above-noted

features taught in Nielsen for the purpose of determining correction values to compensate for

directional components of the offset signal.

However, the combination of Zarubinsky and Nielsen does not expressly disclose a dual

mixer stage radio receiver. The Galal reference teaches a dual mixer stage radio receiver (Figure

18 and Col. 10, line 8 to Col. 11, line 56).

Therefore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to modify the method of Zarubinsky and Nielsen for a dual mixer stage

radio receiver, as taught by Galal, in order to implement a dual path mixing network to provide

for balanced gain and group delay distortion among the upper and lower paths of the mixing network.

As to claim 10, the Zarubinsky reference discloses a method of compensating for DC offset voltages at inputs of in-phase and quadrature phase low pass filters, said method comprising the steps of:

determining a signal delay between the inputs of the low pass filters, said signal delay characterizing in-phase and quadrature phase components of DC offset voltages at the inputs of the low pass filters ("delay stage 207 forwards signal X'_D with a delay of N time slots T. The symbol Z_{-N} is an operator of a Z-transformation. Persons of skill in the art can implement delay stage 207 with out the need of detailed explanation herein, for example, by a shift register. The delay of stage 207 conveniently corresponds to the intrinsic input-to-output delay introduced in in-phase channel 291 (e.g., by DAC 293, LPF 295. This is convenient. As explained in connection with FIG. 3, the "input related" signal X_D is combined with the delayed "output related" X_A (page 5, col. 1, paragraph [0077]));

using the signal delay to separate and define in-phase and quadrature phase multiplication factors associated with the in-phase and quadrature phase DC offsets ("FIG. 9 illustrates a simplified block diagram of offset compensation control loop 401" (page 5, col. 2, paragraph [0094], lines 1-2). "Integrator 441 obtains an estimation of the magnitude and feeds back a compensation offset signal OCOMP (P,P) to either one of the inputs of corresponding digital comparator 221. In the example of FIG. 9, this implemented by subtracting OCOMP (P,P) form ID(P) by subtractor 411. Delay stage 431 delays by the delay time introduced by channel 292" (page 5, col. 2, paragraph [0095]));

incrementally adjusting the signal level of the in-phase component to a more positive or more negative value if the in-phase multiplication factor has a negative or positive value, respectively; and incrementally adjusting the signal value of the quadrature phase component to a more positive or more negative value if the quadrature phase multiplication factor has a negative or positive value, respectively (see page 6, col. 1, paragraphs [0097] and [0098]).

Zarubinsky fails to disclose that the determination of the delay has component delay vectors. However, in an analogous art, Nielsen discloses a receiver including delay measurement means 32 coupled to the demodulator 36 operable to determine delay vectors. See FIG. 2 and col. 4, lines 7-45. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the receiver in Luz by incorporating the above-noted features taught in Nielsen for the purpose of determining correction values to compensate for directional components of the offset signal.

However, the combination of Zarubinsky and Nielsen does not expressly disclose a dual mixer stage radio receiver. The Galal reference teaches a dual mixer stage radio receiver (Figure 18 and Col. 10, line 8 to Col. 11, line 56).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Zarubinsky and Nielsen for a dual mixer stage radio receiver, as taught by Galal, in order to implement a dual path mixing network to provide for balanced gain and group delay distortion among the upper and lower paths of the mixing network.

5.   Claim 9 is rejected under 35 U.S.C. 103(a) as being anticipated by Zarubinsky et al. (U.S.

Patent Application Publication 2002/0114413 A1) in view of Ma et al. (US 4,816,769).

As to claim 9, the Zarubinsky reference discloses a method of setting signal levels of in-

phase and quadrature phase components of a radio receiver between a minimum threshold

voltage and a maximum threshold voltage, the method including setting the gain of an automatic

gain control, increasing the gain of the automatic gain control stage by a predetermined amount

and repeating these steps until the signal levels of the in-phase and quadrature phase components

are greater than or equal to the predetermined minimum threshold value (see page 2, col. 1,

paragraphs [0028], [0030], [0031]; and page 5, col. 2, paragraphs [0089] to [0092]).

Zarubinsky fails to disclose setting the gain to a value at which the signal levels of the in

phase and quadrature phase components are less than or equal to the maximum threshold

voltage, and comparing the signal levels of the in-phase and quadrature phase components to a

predetermined minimum threshold value.

However, in an analogous art, Ma discloses a receiver in which a gain to a value at which

the signal levels of the in phase and quadrature phase components are less than or equal to the

maximum threshold voltage, and comparing the signal levels of the in-phase and quadrature

phase components to a predetermined minimum threshold value. See col. 7, lines 23-42.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention

was made to modify the method in Zarubinsky by including the above-noted features taught in

Ma for the purpose of fine tuning the levels of the in phase and quadrature phase components to

desired values.

Allowable Subject Matter

6.   Claim 7 is allowed.

7.   The following is a statement of reasons for the indication of allowable subject matter:

claim 7 is allowed for the reasons stated in the previous Office action.

Response to Arguments

8.   Applicant's arguments filed 8/21/06 have been fully considered but they are not

persuasive.

Examiner respectfully disagrees with Applicant's arguments.

Regarding claims 2-6, Examiner relies on Luz, not Nielsen, for teaching correcting of in-

phase and quadrature phase DC components. In response to Applicant's arguments against the

references individually, one cannot show nonobviousness by attacking references individually

where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413,

208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir.

1986). Rather, Nielsen is relied on for teaching delay measurement means coupled to the

demodulator operable to determine a delay vector. See FIG. 2 and col. 4, lines 7-45 in Nielsen.

Since Luz already teaches an in-phase and quadrature circuit structure, the <u>combination</u> of Luz

and Nielsen results in the recited elements in a radio receiver, including delay measurement

means coupled to the demodulator operable to determine a delay vector characterizing the in-

phase and quadrature phase DC components.

Regarding claims 8 and 10, Zarubinsky clearly discloses determining a signal delay in

paragraphs 77, 81 and 82. The signal delay must be determined to attain the input-to-output

delay introduced in in-phase channel 291 and the delay N introduced in quadrature channel 292,

for example. Accordingly, Zarubinsky teaches determining a signal delay that characterizes in-

phase and quadrature phase components of a DC offset. Moreover, Zarubinsky teaches using the

determined signal delay to separate and define digital representations of the in-phase DC offset

voltage component and the quadrature phase DC offset voltage component, in paragraph 94,

lines 1-8.

Regarding claim 9, on page 11, line 9 of the 5/19/06 Office action, Examiner clearly

indicated this claim as being rejected under 35 USC 103(a) based on Zarubinsky and Ma.

Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general

allegation that the claims define a patentable invention without specifically pointing out how the

language of the claims patentably distinguishes them from the references. Accordingly,

Applicant must distinguish claim 9 over the combination of Zarubinsky and Ma.

Conclusion

9.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,
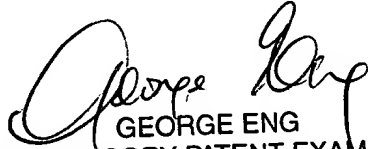
however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Sam Bhattacharya whose telephone number is (571) 272-7917.

The examiner can normally be reached on Weekdays, 9-6, with first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, George Eng can be reached on (571) 272-7495. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sb

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